AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A semiconductor device comprising a driver circuit for supplying a voltage at an output node in accordance with an input signal received at an input node, said driver circuit including:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with voltage of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off complementarily to said first transistor, in accordance with voltage of a second internal node; and

a control circuit controlling voltages of said first and second internal nodes to complementarily turn on said first and second transistors in accordance with the input signal, said control circuit including a voltage adjustment circuit connected to at least one of said first and second internal nodes, and, when the one of said first and second transistors corresponding to the internal node connected to said voltage adjustment circuit is turned on, in accordance with the voltage level of the internal node connected to said voltage adjustment circuit, said voltage adjustment circuit sets said internal node connected to said voltage adjustment circuit at a voltage different from the first and second voltages.

2. (Withdrawn) The semiconductor device according to claim 1, wherein the voltage of said internal node connected to said voltage adjustment circuit is set to one of the first and second voltages when the corresponding transistor is turned on.

3. (Withdrawn) The semiconductor device according to claim 1, wherein

said control circuit includes a timing circuit corresponding to said at least one of said first and second internal nodes, and,

when the transistor corresponding to said internal node connected to said voltage adjustment circuit is turned on, said timing circuit connects one of the first and second voltages to said internal node connected to said voltage adjustment circuit for a predetermined period.

4. (Withdrawn) The semiconductor device according to claim 3, wherein said timing circuit adjusts the predetermined period in accordance with the voltage of said output node.

5. (Withdrawn) The semiconductor device according to claim 3, wherein

said timing circuit includes a delay circuit for delaying the input signal, and

the predetermined period corresponds to delay time of said delay circuit.

6. (Withdrawn) The semiconductor device according to claim 1, wherein

said control circuit sets the internal node of the other of said first and second transistors at one of the first and second voltages for turning on the transistor corresponding to that internal node and to turn off the other of said first and second transistors, and

said control circuit further includes a connection circuit electrically connecting said first internal node to said second internal node for a predetermined period when the transistor corresponding to said internal node is turned on.

7. (Withdrawn) The semiconductor device according to claim 6, wherein

said connection circuit includes a delay circuit delaying the input signal, and

the predetermined period corresponds to delay time of said delay circuit.

8. (Withdrawn) The semiconductor device according to claim 1, wherein said first and second transistors are each first and second field effect transistors having respective gate oxide films, and said semiconductor device further comprises a third field effect transistor having a respective gate oxide film different from said gate oxide film of at least one of said first and second transistors.

9. (Withdrawn) The semiconductor device according to claim 1, wherein said first and second transistors are first and second field effect transistors having respective dielectric films, and said semiconductor device further comprises a third field effect transistor having a dielectric film different from said dielectric film of at least one of said first and second transistors.

10. (Withdrawn) The semiconductor device according to claim 1, wherein

the input signal includes a plurality of signals, and

said control circuit controls the voltages of said first and second internal nodes in accordance with a logic operation result based on the plurality of signals.

11. (Withdrawn) The semiconductor device according to claim 10, wherein

said control circuit further includes a timing circuit connected to at least one of said first and second internal nodes, and

said timing circuit connects one of the first and second voltages on a corresponding one of said first and second transistors transistor to said internal node connected to said voltage adjustment circuit for a predetermined period when said transistor is turned on.

12. (Currently Amended) A semiconductor device comprising a driver circuit for supplying a voltage at an output node in accordance with an input signal received at an input node, said driver circuit including:

a first transistor connected between a first voltage and ~~said~~ the output node, and turned on and off in accordance with voltage level of a first internal node;

a second transistor connected between ~~said~~ the output node and a second voltage, and turned on and off in accordance with voltage level of a second internal node;

a third transistor connected in parallel with said second transistor, between ~~said~~ the output node and the second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage level of ~~said~~ the first internal node; ~~and~~

a control circuit for controlling voltages of ~~said~~ the first and second internal nodes to complementarily turn on said first transistor and said second and third transistors in accordance with the input signal; and

a fourth transistor connected between the second voltage and the second internal node, wherein

said control circuit ~~setting~~ sets one of the first and second voltages for turning on said second and third transistors ~~to said first internal node and to turn~~, turns off said first transistor when said second and third transistors are turned on, and ~~supplying~~ supplies the one of the first and second voltages to ~~said~~ the second internal node for a predetermined period, ~~wherein~~ and

said second transistor has a driving force for supplying the second voltage to ~~said~~ the output node and higher than a driving force of said third transistor.

13. (Currently Amended) The semiconductor device according to claim 12, wherein said control circuit includes a timing circuit ~~corresponding~~ connected to ~~said~~ the second internal node, and ~~said timing circuit adjusts~~ adjusting the predetermined period in accordance with the voltage level of ~~said~~ the output node.

14. (Withdrawn-Currently Amended) The semiconductor device according to claim 12, wherein said control circuit includes a connection circuit for electrically connecting ~~said~~ the first internal node to ~~said~~ the second internal node for the predetermined period.

15. (Withdrawn-Currently Amended) The semiconductor device according to claim 12, wherein

the input signal includes a plurality of signals, and

said control circuit controls the voltages of ~~said~~ the first and second internal nodes in accordance with ~~a result of~~ a logic operation result, based on the plurality of signals.

16. (Currently Amended) The semiconductor device according to claim 12, wherein ~~each of~~ said first, second, ~~and~~ third, and fourth transistors are ~~first, second and third~~ field-effect transistors having respective gate oxide films, and said ~~semiconductor device further comprises a~~ fourth field-effect transistor ~~having~~ has a ~~different~~ gate oxide film having a dielectric constant different from dielectric constant of said gate oxide film of at least one of said first, second, and third transistors.

17. (Withdrawn-Currently Amended) The semiconductor device according to claim ~~12~~ 13, wherein said ~~control~~ timing circuit includes a noise adjustment circuit for supplying one of the first and second voltages for turning on said second and third transistors to ~~said~~ the first internal node in response to an external instruction in a standby state.

18. (Withdrawn) A semiconductor device comprising a first driver circuit and a second driver circuit adjacent each other, each of the first and second driver circuits supplying a voltage at an output node in accordance with an input signal received at an input node, wherein each of said first and second driver circuits includes:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with a voltage of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off in accordance with a voltage of a second internal node;

a third transistor connected in parallel with said second transistor, between said output node and the second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage of said first internal node; and

a control circuit for controlling voltages of said first and second internal nodes to complementarily turn on said first transistor and said second and third transistors in accordance with the input signal, wherein

said control circuit of each of said first and second driver circuits sets one of the first and second voltages for turning on said second and third transistors to said first internal node to turn off said first transistor when said second and third transistors are turned on, and supplies the one of the first and second voltages to said second internal node for a predetermined period,

said second transistor has a driving force for supplying the second voltage to said output node higher than the driving force of said third transistor, and

said control circuit of each of said first and second driver circuits includes a noise adjustment circuit for supplying one of the first and second voltages, for turning on said

second and third transistors, to said second internal node, in accordance with the input signal input to the other driver circuit in a standby state.

19. (New) The semiconductor device according to claim 12, wherein said timing circuit includes fifth and sixth transistors connected in series between the first voltage and the second internal node.

20. (New) The semiconductor device according to claim 19, wherein said timing circuit includes an inverter, said fifth transistor has a control terminal connected to the input node, and said sixth transistor has a control terminal coupled to the output node through said inverter.

21. (New) The semiconductor device according to claim 17, wherein

said timing circuit includes fifth and sixth transistors connected in series between the first voltage and the second internal node, and

said noise adjustment circuit comprises a seventh transistor connected in parallel with said sixth transistor and having a control terminal for receiving the external instruction.